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OPTICAL LOGIC IMPLEMENTATION IN COMPOSITE BILED/BILD CIRCUITS

by

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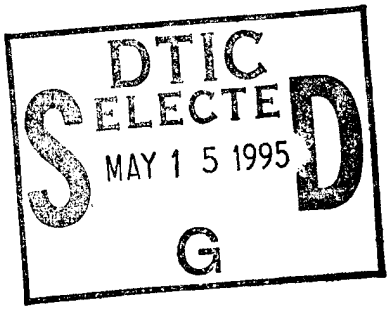

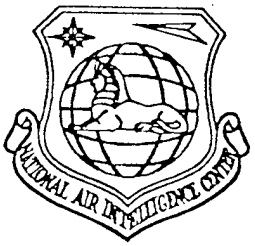

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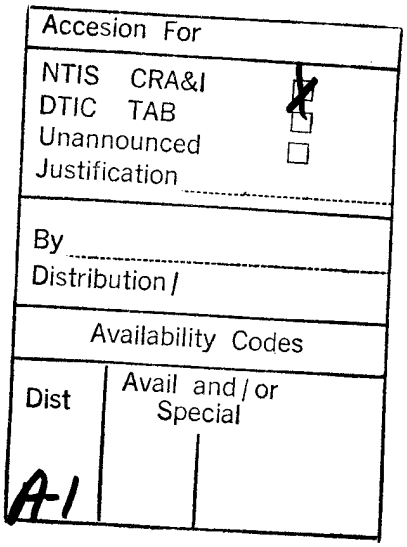

OPTICAL LOGIC IMPLEMENTATION IN COMPOSITE BILED/BILD CIRCUITS

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Liu Shutian Li Chunfei Wu Jie

ABSTRACT Utilizing laser diode or light emitting diode hybrid bi-stable circuit composites, optical multistability and optical XOR logic gates as well as R-S flip-flops have been obtained. This type of optoelectronic logic circuitry and very large scale integrated (VLSI) technology are fully compatible. Because this is the case, it is hoped to apply it to optical information processing, optical signals, and optical computing.

Key Words optical logic gates, optical computing, optical bistability and multistability, optoelectronic hybrid bistable circuit

I. INTRODUCTION

As far as studies of bistable semiconductor laser devices and their logic functions are concerned, in recent years, they have attracted people's attention. Due to the fact that the operating energies of bistable semiconductor laser devices are low, they possess gain characteristics that are compatible with integrated optical circuits. Technologically, they are relatively mature. Thus, as a result, there is the possibility to first achieve applications in other bistable devices in optical communications, optical computing, and other similar realms. In the past several years, people have put forward bistable semiconductor laser devices associated with several types of different mechanisms. For example, optical bistability given rise to because of intra-cavity saturation absorption

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* Numbers in margins indicate foreign pagination. Commas in numbers indicate decimals.

[1,2]; polarization bistability given rise to by differences in TE-TM polarization mode gains caused by thermal stresses in activation layers [3]; as well as optical bistability given rise to by gain saturation characteristics associated with coupled cavities (C^3) [4], and so on, and so on. There is also a type of optoelectronic hybrid bistable semiconductor laser device put forward by people like Chisaikawa Ooromi, et al. Throughout, they use bistable light emitting diodes (BILED) and bistable laser diode (BILD) circuits constructed from light emitting diodes (LED) and laser diodes (LD) as well as photoelectric detectors (PD). Moreover, circuits using BILED demonstrated "and" and "not" as well as optical flip-flops and other such logic components [5-7]. With regard to our first utilization of BILED circuit composites, we simply and conveniently obtained optical multistability, optical XOR logic gates, and optical R-S flip-flops. Thus, using a minimum of separate components, various types of binary system logic gates were completed.

II. OPTICAL MULTISTABILITY ASSOCIATED WITH COMPOSITE BILED CIRCUITS

We discovered in experiments that taking two BILED circuits and connecting them in parallel or series was, in all cases, capable of realizing optical tristability. With parallel connection, the structure is as in Fig.1.

In the Fig., the two left and right sides are, respectively, two BILED circuits. LED's are GaAsP light emitting diodes. PD's are Si optoelectronic triode 3DU32's. Transistor T is used in order to amplify optoelectric currents. V_B is an offset voltage. R_s, R_1, and R_2 are, respectively, current limiting resistances on the main circuit and two branch circuits. R_{11} and R_{12} are used to control opening threshold values for the two BILED circuits. f_1 and f_2 are respectively are optical feedback coefficients associated with $BILED_1$ and $BILED_2$. Two directly

modulated light emitting diodes act as input lights P_i, P_0, P_{01}, and P_{02}. Giving consideration to the nearly linear relationship between LED light output and drive current, input and output signals are capable of being directly obtained from signal voltages at the two ends of the current limiting resistances.

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Taking the electric currents associated with the various branches in the circuit, they are respectively represented by I, I_1, I_2, Id_1, and Id_2. Because of this, one has

$$I = I_1 + I_2 + Id_1 + Id_2,$$
$$I = I(V_B, R_s, R_1, R_2, P_i).$$

In normal situations, Id_1 and Id_2 are only 10-100 μA. In analysis, it is possible to ignore them. Thus, one writes

$$I \approx I_1 + I_2,$$
$$I = I(V_B, R_s, R_1, R_2, P_i).$$

If, in the two bistable circuits, there is only one operating in the upper stable state--for example $BILED_1$--at this time, PD_1-T is saturated,

$$I_{1s} \approx V_B/(R_s + 2R_{LED} + R_1 + R_{ce}) = I_{s0}$$

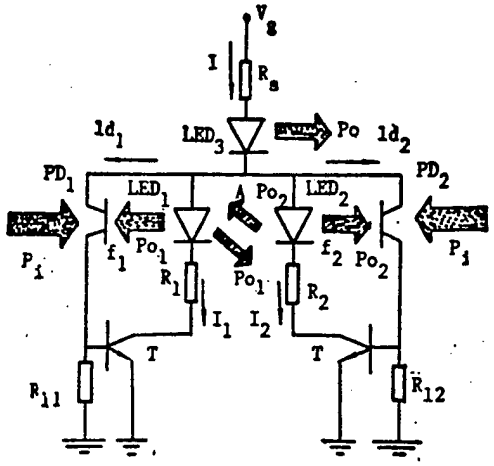

Fig.1 Diagram of optical tri-stable circuit

In this, I_{1s} and I_s are, respectively, saturation values for I_1 and I. At this time, nonlinear components have already been taken and linearized. In conjunction with this, equivalents are resistances. If the two bistable circuits are both operating in the upper stable state, the entire circuit resistance is reduced to

$$R \approx R_s + (R_1 + R_{LED} + R_{on}) \,/\!/\, (R_2 + R_{LED} + R_{on}) + R_{LED_0}$$

At this time, saturation currents $I'_s > I_s$. Moreover, in the $BILED_1$ circuit, due to a reduction in the electrical potential at point A, one gets saturation current $I'_{1s} < I_{1s}$. As is shown in Fig.2, in situations without optical feedback, as far as I and I_1 are concerned, during independent operation of one BILED and simultaneous operation of two BILED, saturation currents are related to changes in input light strength.

Due to the shunt effects of R_{11} and R_{12}, selecting appropriate R1 values, it is possible to control the opening threshold values associated with BILED. As in Fig.3, when R_{11} is reduced, in $BILED_1$ circuit, I_1--in situations without optical feedback--follows the P_i change curve and moves toward the right, thus causing the threshold values to increase.

Selecting $R_{12} < R_{11}$ and, thus, $P_{on2} > P_{on1}$, among these, P_{on1} and P_{on2} are, respectively, $BILED_1$ and $BILED_2$ opening threshold values. Following along with two instances of upward jumps in $BILED_1$ and $BILED_2$, outputs P_0 and P_{01} follow changes in Pi and all form three stable states. See Fig.4 (a), (b), and (c).

In the tristable circuit shown in Fig.1, the third stable state of P_{01} is situated between the second stable state and the low state. Moreover, the third stable state is greater than the second stable state. These two types of different output characteristics are capable of being used respectively in binary

system logic and multiple value logic designs. Optical binary system XOR logic gates and optical R-S flip-flops are the very ones which utilize Pol output characteristics. Moreover, P_0 is capable of making multivalue output responses in multiple value signal inputs. The effect is similar to the "current mirror" associated with I^2L circuits. Thus, it is possible to use them as basic components to design optical multiple value logic gates.

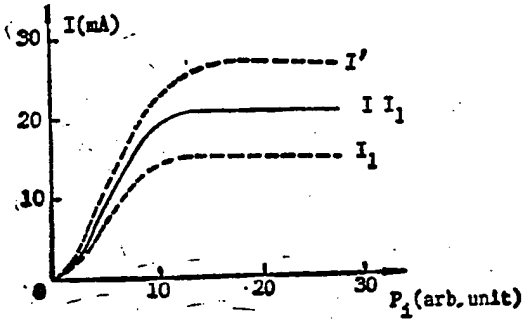

Fig 2 I-P_i and I_1-P_i curves for only BILED works (soild line) and for BILED and BILED work together (dashed line)
V_s=4.0 V, R_i=50 Ω, R_1=R_2=20 Ω, R_{11}=R_{12}=∞

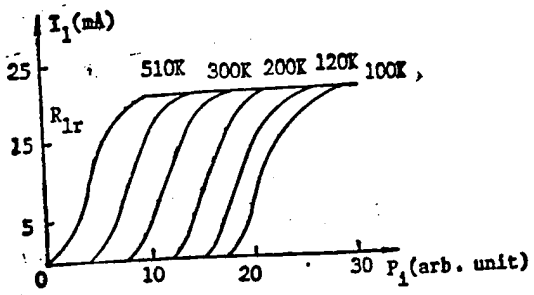

Fig. 3 I_1-P_i curve for different values of R (without optical feedback)
V_s=4.0 V, R_i=50 Ω, R_1=20 Ω

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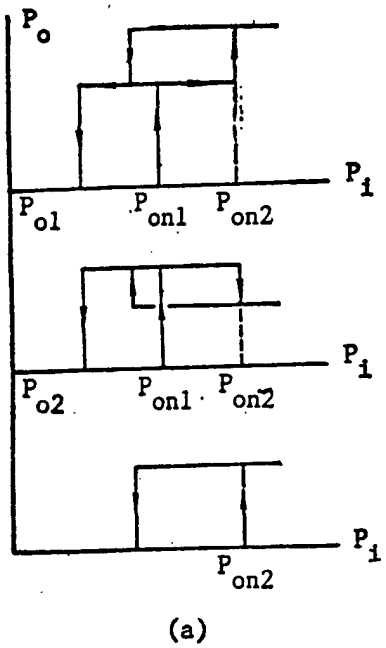


(a)

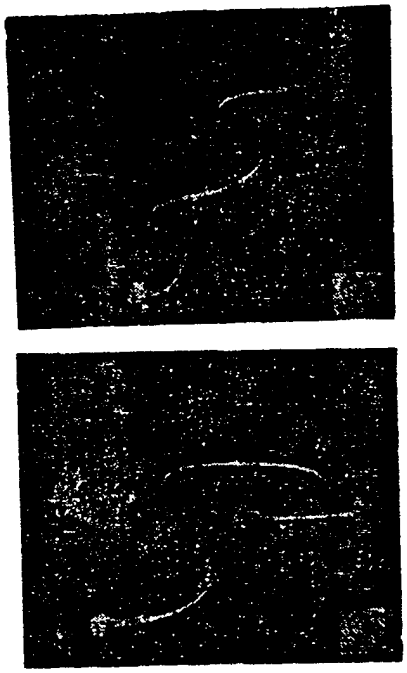
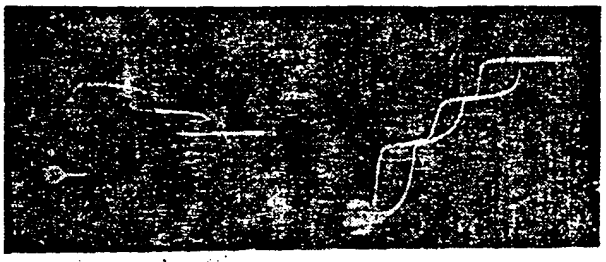


Fig. 4

(a) The hysteresis loop of the output vs. input.
(b), (c) Experimental results, V_s=5.5 V, R_i=50 Ω, R_1=20 Ω, R_2=10 Ω, R_{11}=510 kΩ, R_{12}=200 kΩ



(a) (b)

Fig. 5 Experimental results of multistable circuit which consists of three BILED's in parallel

Multiple optical steady states with even more levels are capable of being achieved by connecting multiple BILED circuits together in parallel.

For example, Fig.5 is the experimental result associated with four stable states constructed from three BILED circuits.

Multiple optical steady states, in the same way, are also capable of being obtained by connecting BILED circuits in series. For example, the three steady state circuit shown in Fig.6(a). The feedback terminals of $BILED_2$ and resistance R3 are connected in parallel to the grounding terminal of $BILED_1$. The function of R3 is to be the $BILED_1$ current supply circuit when $BILED_2$ has not yet opened. Making $R_{11} > R_{12}$, the result is that, following along with the upward jumps of $BILED_1$ and $BILED_2$ one after the other at different light strengths, P_{01} follows P_i in presenting three steady states. See Fig.6(b).

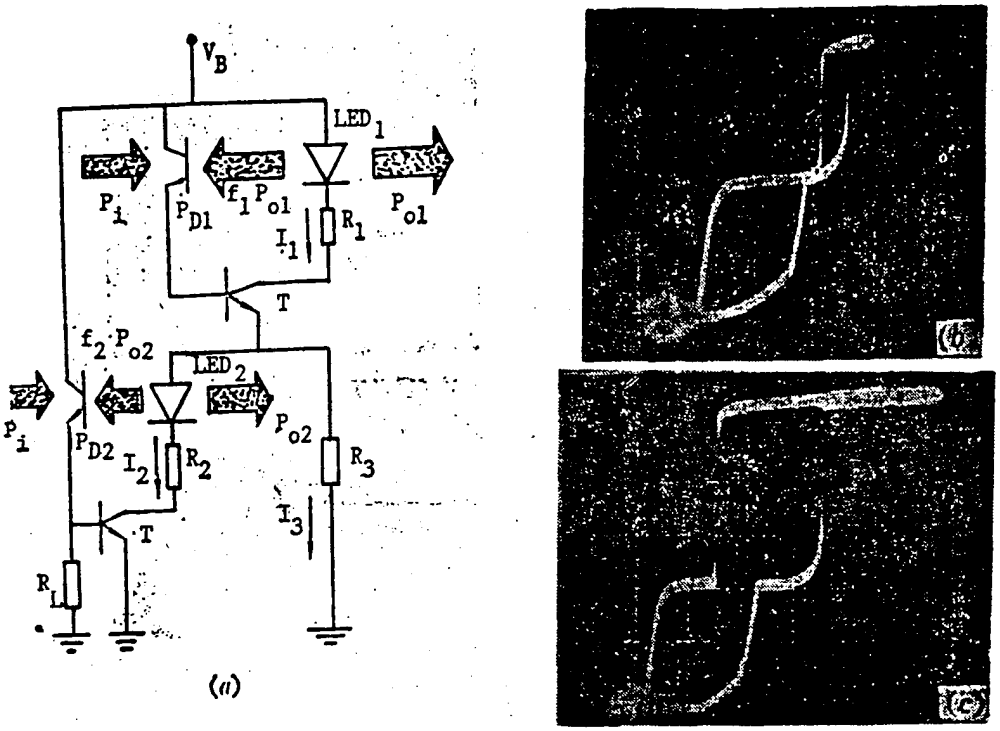


Fig. 6

(a) Diagram of tristable circuit which consists of two BILED's in series. (b), (c) Experimental results of multistability; (b) V_B=6.0 V, R_3=300 Ω, R_1=20 Ω, R_2=3 Ω, R_L=510 kΩ; (c) V_B=6.3 V, R_3=400 Ω, R_1=20 Ω, R_2=3 Ω, R_L=300 kΩ

III. OPTICAL XOR LOGIC GATES AND OPTICAL R-S FLIP-FLOPS

1. Optical XOR Logic Gates

For an optical XOR logic gate constructed from the parallel connection of two BILED circuits, see Fig.7. The Fig. in question and Fig.1 are basically the same. The difference is that the input light strength P_i uses two input square wave signals as substitutes. In conjunction with this, in BILED$_1$, a diode is added to act as a clipper position, causing the output P_{01}, when in the low state, to be very small.

As provided above, in the tristable circuit constructed in Fig.1, the value of the third steady state associated with the

output light strength P_{01} is lower compared to the second steady state value. The difference value $\Delta I_1 = I_{1s} - I'_{1s}$ and offset

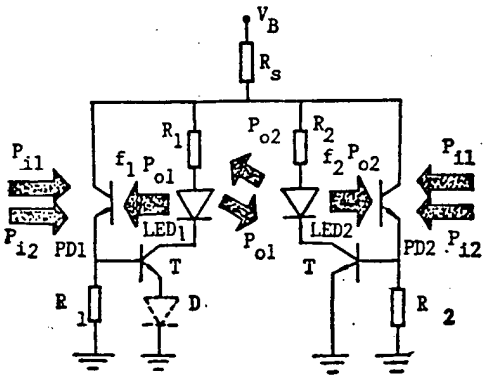


Fig.7 Diagram of optical XOR gate

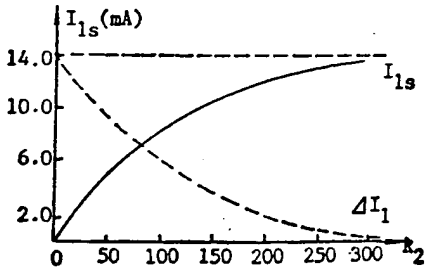


Fig.8 I'_{1s}-R_2 and ΔI_1-R_2 curves, V_B=4.0V, R_s=50Ω, R_1=20Ω

values are related to resistance distributions associated with various branch circuits. When V_B = 4.0V, R_s = 50 ohms, and R_1 = 20 ohms, I_{1s} = 14mA. Fixing R_1 = 20 ohms and changing R2, the relationship curves for delta I_1 and I'_{1s} to R_2 are as shown in Fig.8. When R_2 = 0, I'_{1s} approximately equals 0.8mA which is already very close to the low state. Fig.9(a) is the change loop for P_{01} following P_i when the input light P_i is a triangle wave. When R_2 = 0, the third steady state can be recognized as coinciding with the low state. From the Fig. in question, it is possible to clearly understand operational processes of optical XOR logic gates. When $P_{i1} = P_{i2} = 0$, $BILED_1$ is not able to open. P_{01} = 0. When one of P_{i1} or P_{i2} is 1, $BILED_1$ opens. At this time, P_{01}=1. Moreover, when $P_{i1} = P_{i2} = 1$, $BILED_2$ opens, and BILED1 closes. P_{01} = 0. Thus, XOR logic operation is completed. Fig.9(b) gives optical XOR logic gate input and output wave forms. In the Fig., input signals are a superposition of two low frequency electrical signals.

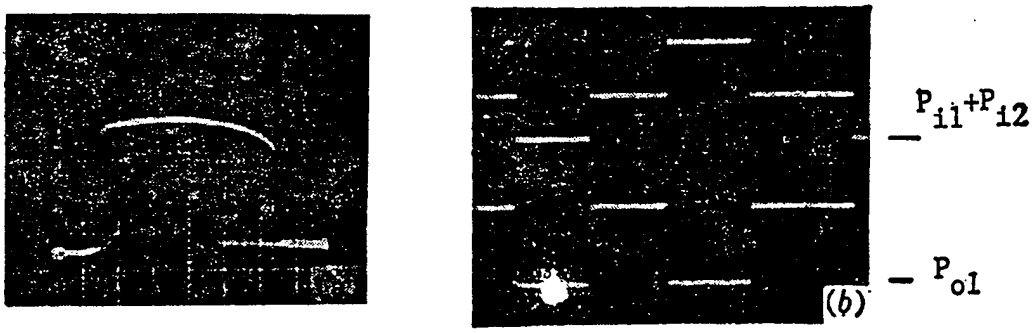


Fig. 9

(*a*) Characteristic loop of output P_0 vs. a triangle wave input P_i.
(*b*) Input-output waveform. V_g=4.0V, E_s=50Ω, E_1=20Ω, E_2=0, E_{i1}=510kΩ, E_{i2}=120kΩ

2. Optical R-S Flip-Flops

Chisaikawa Ooromi, et al, went through the use of two phase inverters (that is, "not" gates) to construct an optical R-S flip-flop. Experimental verification only used two BILED circuits connected in parallel. It was also possible to obtain optical R-S flip-flops. The structure and optical XOR logic gates are basically the same. What is different is that input light signals R and S are replacements respectively. Besides this, $BILED_1$'s output P_{01} is used as optical R-S flip-flop Q_n output. Moreover, $BILED_2$ output P_{02} is used as flip-flop $\overline{Q}_n$ output. On $BILED_1$ input terminals, there are two signals R and $\overline{Q}_n$. Moreover, on $BILED_2$ input terminals, the two signals are S and Q_n. At the same time, we respectively add to the two input terminals two fixed exterior sustained lights H_1 and H_2. Looking at Fig.10(a), when input light is one triangle wave, P_{01} follows P_i, and there is a loop such as that shown in Fig.9(a). Increasing f_1 and f_2, it is possible to make $BILED_2$ and $BILED_2$ jump down threshold values adequately small. If R = 1 and S = 0, $BILED_1$ opens. $Q_n = 1$ and $\overline{Q}_n = 0$. If R = 0 and S = 1, due to the fact that $Q_n = 1$, as a result, it makes $BILED_2$ open. $\overline{Q}_{n+1} = 1$ and $Q_{n+1} = 0$. When R = 0 and S = 0, if the original configuration was in $Q_n = 1$ and

$\overline{Q}_n = 0$ states, due to the sustained light, $H_1 > P_{off1}$ causes $BILED_1$ to still be in the upper state. However, there is need for $H_2 + Q_n < P_{on2}$. Thus, $BILED_2$ will not be able to open. The sustained original state does not change. If the original state is on $Q_n = 0$ and $\overline{Q}_n = 1$, it is only necessary for $H_2 > P_{off2}$.
Moreover, $H_1 + \overline{Q}_n$ is considerably smaller than P_{on1}. This state is also maintained invariable. These types of conditions can be obtained by going through a regulation of R_u and f_i. When $R = S = 1$, it goes without saying that which configuration they will originally be in becomes indeterminate. Fig.10(b) gives optical R-S flip-flop input and output waveforms.

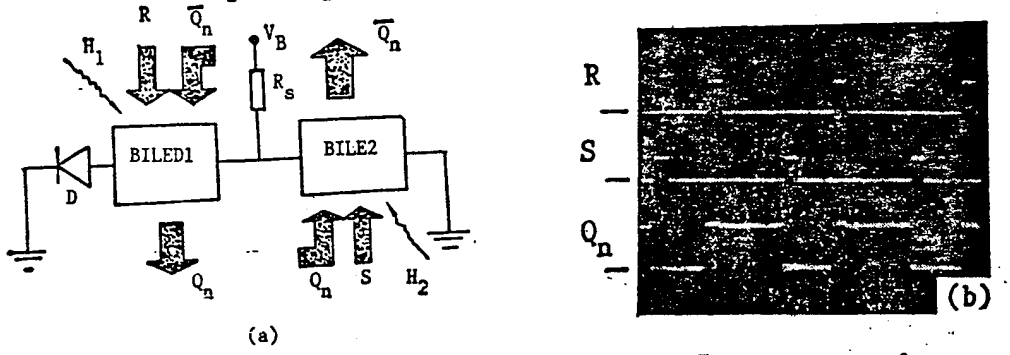


Fig.10 Schematic diagram of an optical R-S flip-flop. Input-output waveform

IV. CONCLUSION

Going through BILED circuit parallel connection and series connection composites, we obtained optical multistability. In conjunction with this, on this foundation, we obtained optical XOR logic gates and optical R-S flip-flops. This type of composite BILED circuit possesses quite great flexibility. (I) It is possible to realize all binary system logic gates. In conjunction with this, it is possible to realize binary system number full additive operations. (II) It is possible to realize, in multivalue logic, several basic logic gates. For optical computing, this undoubtedly possesses great significance.

This type of optoelectronic logic circuit speed is not very fast. It is approximately 200 microseconds. Fast processing optoelectronic logic circuits are capable of using fast response laser diodes or light emitting diodes and avalanche diode APD's for construction. After substitution, this type of optoelectronic logic circuit possesses relatively high response times (approximately 1 ns). At the present time, semiconductor integrated technology, with which industry is already familiar, is capable of making this type of simple, compact optoelectronic logic circuit integration on base plates smaller than 1mm. This will make this type of optoelectronic logic circuit possess broad prospects for applications in optical communications, optical information processing, and optical computing.

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